WE CLAIM:

1. A data communication system for a semiconductor memory system having at least one data path, the data communication system comprising:

a central data path including at least one junction circuit configured for exchanging data signals between the central data path and at least one data path of the at least one data path;

a respective one junction circuit of the at least one junction circuit including means for controlling resetting the respective one junction circuit for preparation of a subsequent data transfer through the respective one junction circuit in accordance with receipt of an input monitor signal indicating that data has been transferred to the respective one junction circuit.

2. The data communication system of Claim 1, wherein the means for controlling resetting prevents resetting of the respective one junction circuit when data is being received by the respective one junction circuit.

3. The data communication system of Claim 1, wherein the data communication system includes a plurality of data banks configured for storing data, and a corresponding data bank of the plurality of data banks is connected to a respective one data path of the at least one data path, the data communication system including:

means for controlling the respective one data path in accordance with receipt of a monitor signal indicating that a data transfer operation has been initiated for transfer of data to the respective one data path, the means for controlling including a means for

generating a control signal for controlling resetting of the respective one data path after data is transferred for preparation of a subsequent data transfer operation.

4. The data communication system of Claim 3, wherein the control signal is provided to the means for generating the control signal as a feedback signal.

5. The data communication system of Claim 1, wherein the input monitor signal indicates that a plurality of data signals are being transferred to the respective one junction circuit, and wherein the respective one junction circuit outputs an output monitor signal indicating that the plurality of data signals are being transferred from the respective one junction circuit.

6. The data communication system of Claim 5, wherein the respective one junction circuit includes a plurality of junction data lines for at least one of processing, receiving and transferring at least one of the input monitor signal, the plurality of data signals, and the output monitor signal.

7. The data communication system of Claim 6, wherein the plurality of junction data lines includes a plurality of input data signal lines and at least one input monitor signal line; and

wherein the respective one junction circuit receives the input monitor signal via an input monitor signal line of the at least one input monitor signal line, and a plurality of

input data signals via a group of input data signal lines of the plurality of input data signal lines.

8. The data communication system of Claim 6, wherein the respective one junction circuit of the at least one junction circuit includes a plurality of output data signal lines and at least one output monitor signal line; and

wherein the respective one junction circuit outputs an output monitor signal via an output monitor signal line of the at least one output monitor signal line; and a plurality of output data signals via the plurality of output data line.

9. The data communication system of Claim 7, wherein the means for controlling resetting controls resetting of the input monitor signal line propagating the input monitor signal and the group of input data signal lines propagating the plurality of input data signals.

10. The data communication system of Claim 7, wherein the respective one junction circuit of the at least one junction circuit includes a plurality of output data signal lines and at least one output monitor signal line;

wherein the respective one junction circuit outputs an output monitor signal via an output monitor signal lines of the at least one output monitor signal line, and a plurality of output data signals via a group of output data signal lines of the plurality of output data signal lines; and

wherein the input monitor signal is received from one of a data path of the

plurality of data paths and the output monitor signal line of another junction circuit of the at least one junction circuit, and the plurality of input data signals is received from one of a data path of the plurality of data paths and the group of output data signal lines of the another junction circuit of the at least one junction circuit.

11. The data communication system of Claim 8, wherein the plurality of junction data lines includes a plurality of input data signal lines and at least one input monitor signal line;

wherein the respective one junction circuit receives the input monitor signal via an input monitor signal line of the at least one input monitor signal line, and a plurality of input data signals via a group of input data signal lines of the plurality of input data signal lines; and

wherein the output monitor signal is transmitted to [one of a data path of the plurality of data paths and] the input monitor signal line of another junction circuit of the at least one junction circuit, and the output data signals are transmitted to [one of a data path of the plurality of data paths and] the group of input data signal lines of the another junction circuit.

12. The data communication system of Claim 6, wherein the means for controlling resetting includes at least one reset circuit included in at least one of the plurality of junction data lines, and a control signal generator for generating a reset control signal which controls the at least one reset circuit.

13. The data communication system of Claim 6, wherein a respective junction data line of the plurality of junction data lines is connected to a discharge circuit for transferring at least one of the received input monitor signal and the plurality of data signals.

14. The data communication system of claim 13, wherein the at least one discharge circuit includes a discharge device;

wherein the means for controlling resetting includes a control signal generator for generating a reset control signal which controls resetting the respective one junction circuit, and a virtual ground signal having a polarity different from the reset control signal; and

wherein the virtual ground signal is applied to the discharge device.

15. The data communication system of Claim 12, wherein feedback signals are provided to the control signal generator.

16. The data communication system of Claim 12, wherein the reset control signal prevents resetting of the plurality of junction data lines when the plurality of data signals and the input junction monitor signal are being received or processed by the junction data lines.

17. The data communication system of Claim 12, wherein the input monitor signal is a pulse signal, and the reset control signal disables the at least one reset circuit for the duration of a pulse of the input monitor signal.

18. The data communication system of Claim 12, wherein the reset circuit is a pre-charge circuit.

19. The data communication system of Claim 12, wherein the reset control signal is a pulse signal generated by a pulse generator.

20. The data communication system as in Claim 21, wherein the pulse generator is triggered by a signal indicative of the input monitor signal.

21. A method for transferring data in a data communication system for a semiconductor memory system having at least one data path comprising the steps of:

connecting a central data path to the at least one data path at a junction circuit;

receiving data in the junction circuit;

processing the data;

transferring the data out of the junction circuit;

resetting of the junction circuit for preparation for receipt of new data; and

controlling the resetting to prevent resetting while the data is being at least one of received and processed.

22. The method of Claim 21, further including the steps of:

receiving an input monitor signal indicating that the data is being transferred to the junction circuit; and

outputting an output monitor signal indicating that the data is being transferred from the junction circuit.

23. The method of Claim 22, wherein the step of controlling further includes the steps of:

generating a reset control signal in accordance with receipt of the input monitor signal; and

controlling via the reset control signal at least one reset circuit associated with data lines receiving data and the input monitor signal.

24. The method of Claim 23, further comprising the steps of generating the reset control signal via a pulse generator; and

triggering the pulse generator by a signal indicative of the input monitor signal.

25. A data communication system for a semiconductor memory system having at least one data path, the data communication system comprising:

means for connecting a central data path to the at least one data path at a junction circuit;

means for receiving data in the junction circuit;

means for processing the data;

means for transferring the data out of the junction circuit;

means for resetting the junction circuit for preparation of receipt of new data; and

means for controlling the resetting to prevent resetting while the data is being at least one of received and processed.

26. The data communication system of Claim 25, further comprising:

means for receiving an input monitor signal indicating that the data is being transferred to the junction circuit; and

means for outputting an output monitor signal indicating that the data is being transferred from the junction circuit.

27. The data communication system of Claim 26, wherein the means for controlling further includes:

means for generating a reset control signal in accordance with receipt of the input monitor signal; and

means for resetting including at least one reset circuit associated with data lines receiving data and the input monitor signal controlled via the reset control signal.

28. The data communication system of Claim 27, wherein the reset control signal is generated via a pulse generator, and further including means for triggering the pulse generator by a signal indicative of the input monitor signal.